



SPECTRUM

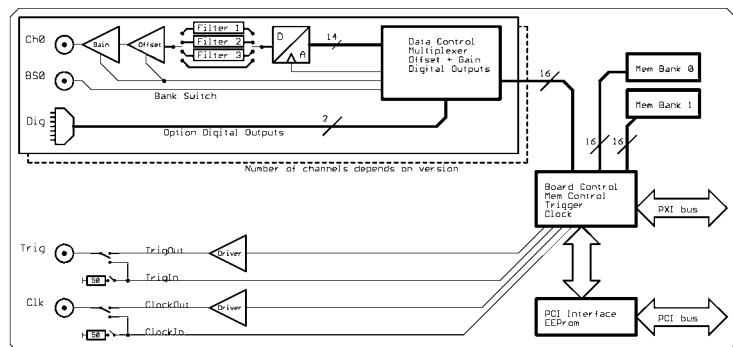
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MX.60xx - 14 bit 125 MS/s Arbitrary Waveform Generator

- **PXI 3U / CompactPCI 3U format**
- **Fast 14 bit arbitrary waveform generator**
- **Models with 20 MS/s, 60 MS/s or 125 MS/s**
- **1 or 2 channel versions**
- **Simultaneous sampling on all channels**
- **Output up to ± 3 V in 50 Ohm**
- **Amplifier option available for ± 10 V**
- **Offset and amplitude programmable**
- **3 software selectable filters**
- **Up to 64 MSample memory**
- **FIFO mode**
- **Bank switching mode**
- **Synchronization possible**
- **Software SPEasyGenerator included**



Hardware block diagram



Product range overview

Model	1 channel	2 channels
MX.6011	20 MS/s	20 MS/s
MX.6021	60 MS/s	60 MS/s
MX.6030	125 MS/s	
MX.6033	125 MS/s	60 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP/Vista/7 drivers
- Linux 32bit and 64bit drivers
- SBench 5.x for Windows
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MX.60xx series offers 4 different versions of arbitrary waveform generators for the CompactPCI bus. With these boards it is possible to generate free definable waveforms on several channels synchronously. There are one or two channels on one board with a maximum sampling rate of 125 MS/s. The internal standard Sync-bus allows the setup of synchronous multi channel systems with higher channel numbers. It is also possible to combine the arbitrary waveform generator with other boards of the MX product family like analogue or digital acquisition boards.

With the up to 64 MSample large on-board memory long waveform can be generated even with high sampling rates. The memory can be used also as a FIFO buffer to make continuous data transfer from PC memory or hard disk.

Software programmable parameters

sampling rate	1 kS/s to max sampling rate, external clock, ref clock, PXI clock
Output amplitude	± 100 mV up to ± 3 V in 1 mV steps (Amp option: ± 333 mV up to ± 10 V)
Output offset	± 3 V selectable in 1 mV steps (Amp option: ± 10 V in 3 mV steps)
Filters	no filter or one of 3 different filters as defined in technical data section
Mode	Singleshot, Continuous, Standard, Bank Switching
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger mode	External, Software, PXI Line[5..0], PXI Startrigger
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Output amplitude	± 100 mV up to ± 3 V in 1 mV steps
Multiple Replay segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is possible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is fed in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. Using a simple software command one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

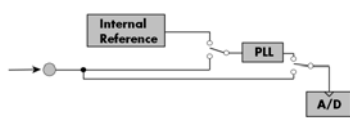
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock

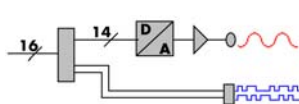


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Bank Switching

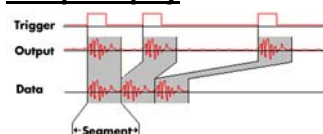
In bank switching mode two different signals of the same length are written in the on-board memory. Controlled by an external bank signal that is individually available for every channel one of the signals is selected for output. The user can define whether the signal should switch immediately or whether the complete signal should be generated up to the end.

Digital outputs



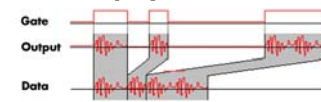
This option outputs additional synchronous digital channels phase-stable with the analog data. When this option is installed there are 2 additional digital outputs for every analog D/A channel.

Multiple Replay



The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.

Gated Replay



The Gated Sampling option allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has a programmed level.

Singleshot output

When singleshot output is activated the data of the on-board memory is replayed exactly one time. As trigger source one can use the external TTL trigger or the software trigger.

Continuous output

When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

± 10 V Amplifier



The amplifier board allows the output of ± 10 V on up to four channels without software modification. The standard outputs of the card are amplified by factor 3.33. The amplifier which has 30 MHz bandwidth has an output impedance of 50 Ohm. This allows ± 10 V with high impedance termination or ± 5 V with 50 ohm termination.

Technical Data

Resolution	14 bit	Dimension	160 mm x 100 mm (Standard 3U)
Integral linearity (DAC)	± 1.5 LSB typ.	Width (Standard)	1 slot
Differential linearity (DAC)	± 1.0 LSB typ.	Width (with digital outputs)	2 slots
Output resistance	< 1 Ohm	Width of Amplifier option	1 slot
Max output swing in 50 Ohm	± 3 V (offset + amplitude)	Analogue connector	3 mm SMB male
Max slew rate (no filter)	> 0.9 V/ns	Digital connector	40 pol half pitch (Hirose FX2 series)
Multi: Trigger to 1st sample delay	fixed	Digital Outputs delay to analog sample	0 samples (due to internal correction)
Multi: Recovery time	< 20 samples	Warm up time	10 minutes
Ext. clock: delay to internal clock	42 ns ± 2 ns	Operating temperature	0°C - 50°C
Output to trigger out delay 1 channel	< 5 MS/s: -5 samples, > 5 MS/s: -21 samples	Storage temperature	-10°C - 70°C
Output to trigger out delay 2 channels	< 5 MS/s: -3.5 samples, > 5 MS/s: -12 samples	Humidity	10% to 90%
Crosstalk @ 1 MHz signal ±3 V	< -80 dB	Offset stepsize	< 2 mV
Output accuracy	< 1%	Amplitude stepsize	< 1 mV
Min internal clock	1 kS/s	Power consumption 3.3 V @ full speed	max. 1.28 A (4.2 Watt)
Min external clock	DC	Power consumption 5 V @ full speed	max. 0.90 A (5.5 Watt)
Trigger input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Clock and Filter

	MX.6011	MX.6021	MX.6030 MX.6033
max internal clock	20 MS/s	60 MS/s	125 MS/s
max external clock	20 MS/s	60 MS/s	125 MS/s
-3 dB bandwidth no filter	> 10 MHz	> 30 MHz	> 60 MHz
Filter 3: Characteristics	4th order Butterworth		5th order Butterworth
Filter 3: -3 dB bandwidth	5 MHz	10 MHz	25 MHz
Filter 2: Characteristics	4th order Butterworth		4th order Butterworth
Filter 2: -3 dB bandwidth	1 MHz	2 MHz	5 MHz
Filter 1: Characteristics	4th order Butterworth		4th order Butterworth
Filter 1: -3 dB bandwidth	100 kHz	200 kHz	500 kHz

Dynamic Parameters

	MX.6011	MX.6011	MX.6011	MX.6021	MX.6021	MX.6030 MX.6033	MX.6030 MX.6033	MX.6030 MX.6033	MX.6030 MX.6033
Test - Samplerate	20 MS/s	20 MS/s	20 MS/s	60 MS/s	60 MS/s	62.5 MS/s	62.5 MS/s	125 MS/s	125 MS/s
Output Frequency	80 kHz	800 kHz	4 MHz	170 kHz	1.7 MHz	400 kHz	4 MHz	400 kHz	4 MHz
Output Level	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V
Used Filter	100 kHz	1 MHz	5 MHz	200 kHz	2 MHz	500 kHz	5 MHz	500 kHz	5 MHz
SNR (typ)	> 61.0 dB	> 60.0 dB	> 54.0 dB	> 61.0 dB	> 59.0 dB	> 60.8 dB	> 53.9 dB	> 60.1 dB	> 54.8 dB
THD (typ)	< -70.1 dB	< -67.1 dB	< -44.5 dB	< -72.2 dB	< -62.1 dB	< -71.2 dB	< -55.4 dB	< -71.2 dB	< -55.6 dB
SFDR (typ), excl harm.	> 83.8 dB	> 70.9 dB	> 59.0 dB	> 80.2 dB	> 67.2 dB	> 80.2 dB	> 65.2 dB	> 70.3 dB	> 65.7 dB

Dynamic parameters are measured at the given output level and 50 Ohm termination with a high resolution data acquisition card and are calculated from the spectrum. The sample rate that is selected is the maximum possible one. All available channels are activated for the tests. SNR and SFDR figures may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range

Order information

Order No	Description	Order No	Description
MX6011	MX.6011 with 8 MSample memory and drivers/SBench 5.x	MX6xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MX6021	MX.6021 with 8 MSample memory and drivers/SBench 5.x	MX6xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MX6030	MX.6030 with 8 MSample memory and drivers/SBench 5.x	MX6xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MX6033	MX.6033 with 8 MSample memory and drivers/SBench 5.x	MX6xxx-up	Additional handling costs for later memory upgrade
MX6xxx-mr	Option Multiple Replay: Memory segmentation	MX6xxx-1Amp	±10 V Amplifier board with 1 channel
MX6xxx-gs	Option Gated Sampling: Gate signal controls replay	MX6xxx-2Amp	±10 V Amplifier board with 2 channels
MX60xx-dig	Additional 2 synchronous digital outputs per channel, incl. cable	MX6xxx-4Amp	±10 V Amplifier board with 4 channels
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	MX60xx-dl	DASYLab driver for MX.60xx series
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	MX60xx-hp	VEE driver for MX.60xx series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	MX60xx-lv	LabVIEW driver for MX.60xx series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.

Technical changes and printing errors possible