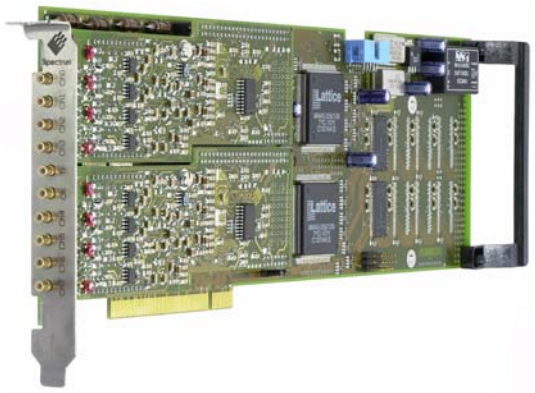
SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MI.31xx - 8 channel 12 bit A/D up to 25 MS/s

- **Standard PCI format**
- **12 bit A/D converter board**
- **1 MS/s, 10 Ms/s or 25 MS/s**
- **2, 4 or 8 channels per board**
- **Simultaneously sampling on all channels**
- **8 input ranges: ±50 mV up to ± 10 V**
- **Up to 256 MSample memory**
- **FIFO mode to RAM or hard disk**
- **Window and Pulsewidth trigger**
- **Input offset up to ±100%**
- **Synchronization possible**
- **Software SBench for Windows included**
- **Software SBench for Linux included**



Product range overview

Model	1 channel	2 channels	4 channels	8 channels
MI.3110	1 MS/s	1 MS/s		
MI.3111	1 MS/s	1 MS/s	1 MS/s	
MI.3112	1 MS/s	1 MS/s	1 MS/s	1 MS/s
MI.3120	10 MS/s	10 MS/s		
MI.3121	10 MS/s	10 MS/s	10 MS/s	
MI.3122	10 MS/s	10 MS/s	10 MS/s	10 MS/s
MI.3130	25 MS/s	25 MS/s		
MI.3131	25 MS/s	25 MS/s	25 MS/s	
MI.3132	25 MS/s	25 MS/s	25 MS/s	25 MS/s

Software/Drivers

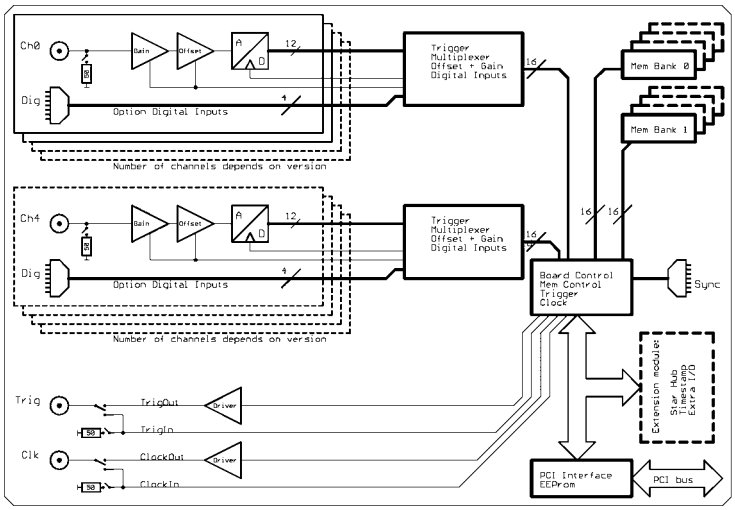
A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP/Vista/7 drivers
- Linux 32bit and 64bit drivers
- SBench 5.x for Windows
- SBench 6.x Base version for Windows and Linux
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MI.31xx series allows recording of two, four or eight channels with samplerates of 1 MS/s, 10 MS/s or 25 MS/s. Due to the proven design a wide variety of 12 bit A/D converter boards for PCI bus could be offered. These boards are available in several versions and different speed grades making it possible for the user to find an individual solution.
As an option 4 digital inputs per channel could be recorded synchronously. The installed memory of up to 256 MSample will be used for fast data recording. It can completely be used by the currently active channels. If using slower samplerates the memory is switched to a FIFO buffer and data will be transferred online to the PC memory or to hard disk.

Hardware block diagram

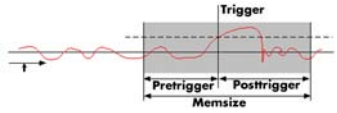


Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock
Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/256 to 255/256 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

Input impedance
All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode


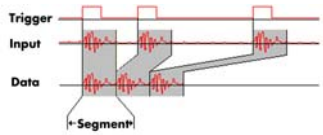
The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

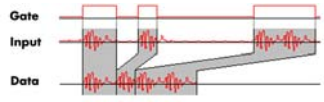
Channel trigger
The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

External trigger I/O
All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

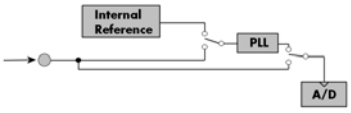
Multiple Recording


The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

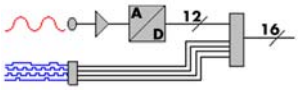
Gated Sampling


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

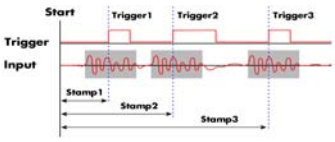
Digital inputs


This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

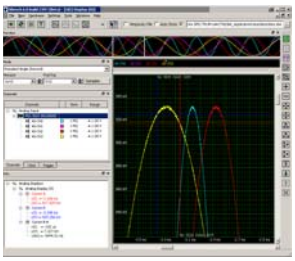
Cascading
The cascading option synchronises up to 4 Spectrum boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star-Hub
The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp


The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

SBench 6

A base licence of SBench 6 the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. Using the base license ist is possible to test the card and to show acquired data. There are also some basic measurement functions included in the base license. The card comes with a demo license for the professional version giving the user the oportunity to test the features of the professional version with the new hardware. Existing customers have the oportunity to request a demo license for the professional version at Spectrum. The professional version contains several new measurement functions, FFT, import and exporr (including MATLAB and ASCII) as well as the streaming modes. The data streaming modes allow to continuously acquire data to hard disk. SBench 6 has been optimized to handle data files of several GByte. More details on SBench 6 are found in the dedicated SBench 6 data shett. The version 6 is running under Windows as well as under Linux (KDE and GNOME). A test version of SBench 6 is freely available in the internet. This test version will also operate with demo cards and can be tested as Professional version without any hardware installed.

Technical Data

Resolution	12 bit	Dimension	312 mm x 107 mm
Differential linearity error	≤ 1 LSB (ADC)	Width (Standard)	1 full size slot
Integral linearity error	≤ 2.5 LSB (ADC)	Width (with digital inputs)	1 full size slot and 1 half size slot
Multi: Trigger to 1st sample delay	fix	Connector	3 mm SMB male
Multi: Recovery time	< 20 samples	Input impedance	50 Ohm / 1 MOhm || 25 pF
ext. Trigger accuracy	1 Samples	Overvoltage protection (range ≤ ±1 V)	±5 V
int. Trigger accuracy	1 Sample	Overvoltage protection (range > ±1 V)	±50 V
Ext. clock: delay to internal clock	42 ns ±2 ns	Warm up time	10 minutes
input signal with 50 ohm termination	max 5 V rms	Operating temperature	0°C - 50°C
Digital Inputs input impedance	110 Ohm @ 2.5 V	Storage temperature	-10°C - 70°C
Digital Inputs delay to analog sample	-4 samples	Humidity	10% to 90%
Min internal clock	1 kS/s	Power consumption 5 V @ full speed	max 3.3 A (16.5 Watt)
Min external clock	1 kS/s	Power consumption 5 V @ power down	max 2.5 A (12.5 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Input range	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V	±10 V
Software programmable offset	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V	±10 V
Offset error	< 1 LSB, adjustable by user							
Gain error	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %
Noise (rms): 50 Ohm, 25 MS/s	< 1.5 LSB	< 1.2 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB
Crosstalk 500 kHz signal, ±50 mV input, 50 Ohm	< -70 dB							

Dynamic Parameters

	MI.3110 MI.3111	MI.3112	MI.3120 MI.3121	MI.3122	MI.3130 MI.3131	MI.3132
max internal clock	1 MS/s	1 MS/s	10 MS/s	10 MS/s	25 MS/s	25 MS/s
max external clock	1 MS/s	1 MS/s	10 MS/s	10 MS/s	25 MS/s	25 MS/s
-3 dB bandwidth	> 500 kHz	> 500 kHz	> 5 MHz	> 5 MHz	> 12.5 MHz	> 12.5 MHz
Test - Samplerate	1 MS/s	1 MS/s	10 MS/s	10 MS/s	25 MS/s	25 MS/s
Testsignal frequency	90 kHz	90 kHz	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	> 68.2 dB	> 67.5 dB	> 65.5 dB	> 65.4 dB	> 63.5 dB	> 62.8 dB
THD (typ)	< -62.8 dB	< -62.8 dB	< -62.5 dB	< -62.5 dB	< -62.5 dB	< -62.5 dB
SFDR (typ), excl harm.	> 80.8 dB	> 80.5 dB	> 80.5 dB	> 78.5 dB	> 79.5 dB	> 79.3 dB
SINAD (typ)	> 61.7 dB	> 61.5 dB	> 60.7 dB	> 60.7 dB	> 60.0 dB	> 59.6 dB
ENOB (based on SINAD)	10.0	9.9	9.8	9.8	9.7	9.6

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MI3110	MI.3110 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MI3111	MI.3111 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MI3112	MI.3112 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MI3120	MI.3120 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-128M	Option: 128 MSample memory instead of 8 MSample standard mem
MI3121	MI.3121 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-256M	Option: 256 MSample memory instead of 8 MSample standard mem
MI3122	MI.3122 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-up	Additional handling costs for later memory upgrade
MI3130	MI.3130 with 8 MSample memory and drivers/SBench 5.x		
MI3131	MI.3131 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-mr	Option Multiple Recording: Memory segmentation
MI3132	MI.3132 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-gs	Option Gated Sampling: Gate signal controls acquisition
		MI3xxx-dig	Additional 4 synchronous digital inputs per channel, incl. cable
MI3xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system		
MIxxxx.xio	Extra I/O, internal connector: 16 DI/O, 4 Analog out	MI31xx-dl	DASYLab driver for MI.31xx series
MI3xxx-time	Timestamp option: Extra memory for trigger time	MI31xx-hp	VEE driver for MI.31xx series
MIxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	MI31xx-lv	LabVIEW driver for MI.31xx series
MI3xxx-cs	Synchronisation of 2 - 4 boards, one option per system	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm

Technical changes and printing errors possible