



SPECTRUM

SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MC.40xx - 14 bit transient recorder

- CompactPCI 6U format
- Fastest 14 bit A/D converter board
- Models with 20 MS/s or 50 MS/s
- 1, 2 or 4 channels acquisition
- Simultaneously sampling on all channels
- 6 input ranges: ± 200 mV up to ± 10 V
- Up to 256 MSample memory
- FIFO mode
- Window and pulsewidth trigger
- Input offset up to $\pm 200\%$
- Software SBench for Windows included
- Software SBench for Linux included



Product range overview

Model	1 channel	2 channels	4 channels
MC.4020	20 MS/s		
MC.4021	20 MS/s	20 MS/s	
MC.4022	20 MS/s	20 MS/s	20 MS/s
MC.4030	50 MS/s		
MC.4031	50 MS/s	50 MS/s	
MC.4032	50 MS/s	50 MS/s	50 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

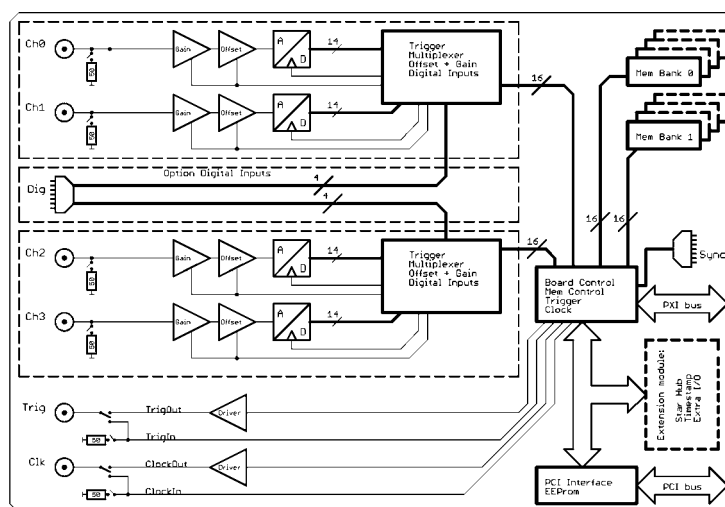
- Windows 98/ME/NT/2000/XP/Vista/7 drivers
- Linux 32bit and 64bit drivers
- SBench 5.x for Windows
- SBench 6.x Base version for Windows and Linux
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MC.40xx is best suitable for applications that need high sampling rates as well as a maximum signal dynamic. These boards offer a resolution 4 times higher than 12 bit boards. On the MC.40xx every channel has its own amplifier and A/D converter. Each input channel can be adapted to a wide variety of signal sources. This is done by software selecting a matching input range, an input impedance and an individual input offset. The user will find easily a matching solution from the six offered models. These versions are working with sampling rates of 20 MS/s or 50 MS/s and have one, two or four channels and can also be updated to a multi-channel system using the internal synchronization bus. Data is written in the internal 8 MSamples up to 256 MSample large memory. This memory can also be

used as a FIFO buffer. In FIFO mode data can be transferred on-line directly into the PC RAM or to hard disk.

Hardware block diagram



Software programmable parameters

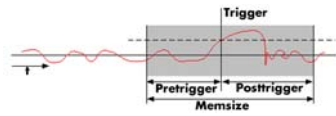
sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Input Range	± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	$\pm 200\%$ in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/1024 to 1023/1024 of input range (10 bit)
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

Input impedance

All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected.

After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsizel - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

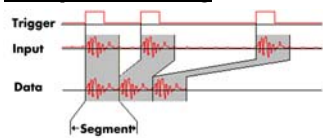
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

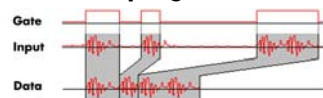
Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The

on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling



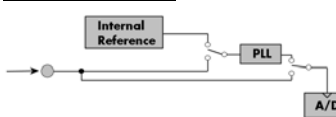
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a pro-

grammed level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

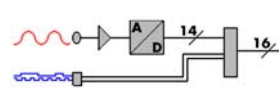
Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the board for high-quality mea-

surements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 2 additional digital inputs for every analog A/D channel.

Cascading

The cascading option synchronises up to 4 Spectrum boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

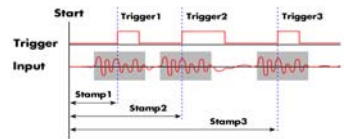
Star-Hub

The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

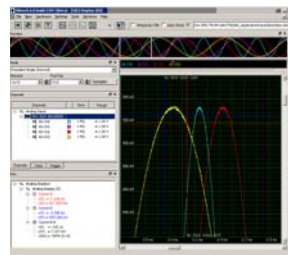
Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time,

externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

SBench 6



A base licence of SBench 6 the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. Using the base license ist is possible to test the card and to show acquired data. There are also some basic measurement functions included in the base license. The card comes with a demo license for the professional

version giving the user the opportunity to test the features of the professional version with the new hardware. Existing customers have the opportunity to request a demo license for the professional version at Spectrum. The professional version contains several new measurement functions, FFT, import and exporr (including MATLAB and ASCII) as well as the streaming modes. The data streaming modes allow to continuously acquire data to hard disk. SBench 6 has been optimized to handle data files of several GByte. More details on SBench 6 are found in the dedicated SBench 6 data shett. The version 6 is running under Windows as well as under Linux (KDE and GNOME). A test version of SBench 6 is freely available in the internet. This test version will also operate with demo cards and can be tested as Professional version without any hardware installed.

Technical Data

Resolution	14 bit	Dimension	160 mm x 233 mm (Standrad 6U)
Differential linearity error	± 0.5 LSB typ. (ADC)	Width (Standard)	1 slot
Integral linearity error	± 1 LSB typ (ADC)	Width (with digital inputs)	2 slots
Multi: Trigger to 1st sample delay	fixed	Width (with star hub option)	2 slots
Multi: Recovery time	< 20 samples	Analogue Connector	3 mm SMB male
ext. Trigger accuracy	1 Sample	Digital Connector	40 pol half pitch (Hirose FX2 series)
int. Trigger accuracy	1 Sample	Digital Inputs delay to analog sample	-6 samples
Ext. clock: delay to internal clock	42 ns ± 2 ns	Overvoltage protection (range ≤ ±1 V)	±5 V
input signal with 50 W termination	max 5 V rms	Overvoltage protection (range > ±1 V)	±50 V
Trigger output delay	1 Sample	Warm up time	10 minutes
Input impedance	50 Ohm / 1 MOhm 25 pF	Operating temperature	0°C - 50°C
Crosstalk 1 MHz sine signal 50 Ohm	< -80 dB	Storage temperature	-10°C - 70°C
Crosstalk 1 MHz sine signal 1 MOhm	< -65 dB	Humidity	10% to 90%
Min internal clock	1 kS/s	Zero offset error	adjustable by user
Min external clock	500 kS/s	Gain error	< 1 % of full scale
		Power consumption 3.3 V @ full speed	max. 1.57 A (5.2 Watt)
		Power consumption 5 V @ full speed	max. 1.91 A (9.6 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	MC.4020 MC.4021	MC.4022	MC.4030 MC.4031	MC.4032
max internal clock	20 MS/s	20 MS/s	50 MS/s	50 MS/s
max external clock	20 MS/s	20 MS/s	50 MS/s	50 MS/s
-3 dB bandwidth	> 10 MHz	> 10 MHz	> 25 MHz	> 25 MHz
Zero noise level at 50 Ohm	< 2.1 LSB rms	< 2.6 LSB rms	< 2.9 LSB rms	< 3.6 LSB rms

Dynamic Parameters

	MC.4020 MC.4021	MC.4022	MC.4030 MC.4031	MC.4032
Test - Samplerate	20 MS/s	20 MS/s	50 MS/s	50 MS/s
Testsignal frequency	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	> 70.3 dB	> 70.1 dB	> 67.1 dB	> 65.5 dB
THD (typ)	< -73.0 dB	< -73.0 dB	< -72.8 dB	< -72.8 dB
SFDR (typ), excl harm.	> 82.8 dB dB	> 82.3 dB	> 75.8 dB	> 75.2 dB
SINAD (typ)	> 68.4 dB	> 68.3 dB	> 66.1 dB	> 64.8 dB
ENOB (based on SINAD)	> 11.1	> 11.1	> 10.7	> 10.5

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MC4020	MC.4020 with 8 MSample memory and drivers/SBench 5.x	MC4xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MC4021	MC.4021 with 8 MSample memory and drivers/SBench 5.x	MC4xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MC4022	MC.4022 with 8 MSample memory and drivers/SBench 5.x	MC4xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MC4030	MC.4030 with 8 MSample memory and drivers/SBench 5.x	MC4xxx-128M	Option: 128 MSample memory instead of 8 MSample standard mem
MC4031	MC.4031 with 8 MSample memory and drivers/SBench 5.x	MC4xxx-256M	Option: 256 MSample memory instead of 8 MSample standard mem
MC4032	MC.4032 with 8 MSample memory and drivers/SBench 5.x	MC4xxx-up	Additional handling costs for later memory upgrade
MC4xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	MC4xxx-mr	Option Multiple Recording: Memory segmentation
MC4xxx-time	Timestamp option: Extra memory for trigger time	MC4xxx-gs	Option Gated Sampling: Gate signal controls acquisition
MCxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	MC40xx-dig	Additional 4 synchronous digital inputs per channel, incl. cable
		MC4xxx-cs	Synchronisation of 2 - 4 boards, one option per system
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	MC40xx-dl	DASYLab driver for MC.40xx series
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	MC40xx-hp	VEE driver for MC.40xx series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	MC40xx-lv	LabVIEW driver for MC.40xx series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.

Technical changes and printing errors possible